MICRONAS

MAS 7825

FFSK modem

APPLICATION

- FFSK modem function for NMT mobile phones and base stations
- Suitable for NMT 450 and 900 systems
- General purpose applications

FEATURES

- Full duplex 1200 baud FFSK modem
- Build in frame synchronization
- Long and short frame capability
- Build in USART function
- Bus compatible with most microprocessors
- Single + 5 V supply voltage
- Low power consumption 10 mW typically
- Available in 28 pin PLCC

GENERATION DESCRIPTION

MAS7825 is a complete single chip 1200 baud FFSK modem for NMT system. IC needs minimum number of external components. The modem contains bit and frame synchronization, transmitter and receiver frame counters, two 8-bit parallel - serial registers for the transmitted and received data plus status and control registers. The microprocessor interface is made with the 8-bit bus and control lines. Build-in crystal oscillator performs all necessary timing functions.

Microprocessor Interface

Flexible use of control lines maximizes an easy interfacing to various microprocessor systems. CPU can read status and data registers and write to control and data registers. Interrupt - based data transfer minimizes CPU loading.

Clock Circuit

The build-in chrystal oscillator (3,6864 MHz) is used to generate all necessary frequencies in modem operation. Clock circuit can also be used with an external clock signal connected to OSC IN pin. The 19,2 kHz frequency output is available for external use.

Transmitter

Transmitter operation is totally independent of receiver. Transmitting will start immediately after loading a byte to data register. If transmitter interrupt is enabled MAS7825 requires a new byte by interrupting the CPU till whole frame has been sent. During transmit operation CPU can monitor the operation of the modem by reading the status register.

Transmitted byte is sent bit by bit to modulator which activates a counter with certain frequency specified by the bit state. Output of the counter is then fed to 7 bit D/A converter to produce sine wave with mark/space frequency.

Receiver

Demodulator converts the received digitalized FFSK signal to data bytes in data register. Detection is made by delay detection method. After that data flow is filtered with digital low pass filter. Bit synchronization is made with phase locked loop (PLL). After synchronizing to bit flow (15 bits) frame synchronization pattern will be searched. After synchronizing to frame MAS7825 converts all received bits to bytes in data register including the subsequent bit and frame sync bits.

P.O.Box 51, Kamreerintie 2, SF-02771 Espoo, Finland Tel. Int. +358-0-80521, Fax +358-0-8053213, Telex 1000691, Teletex 244-1000691

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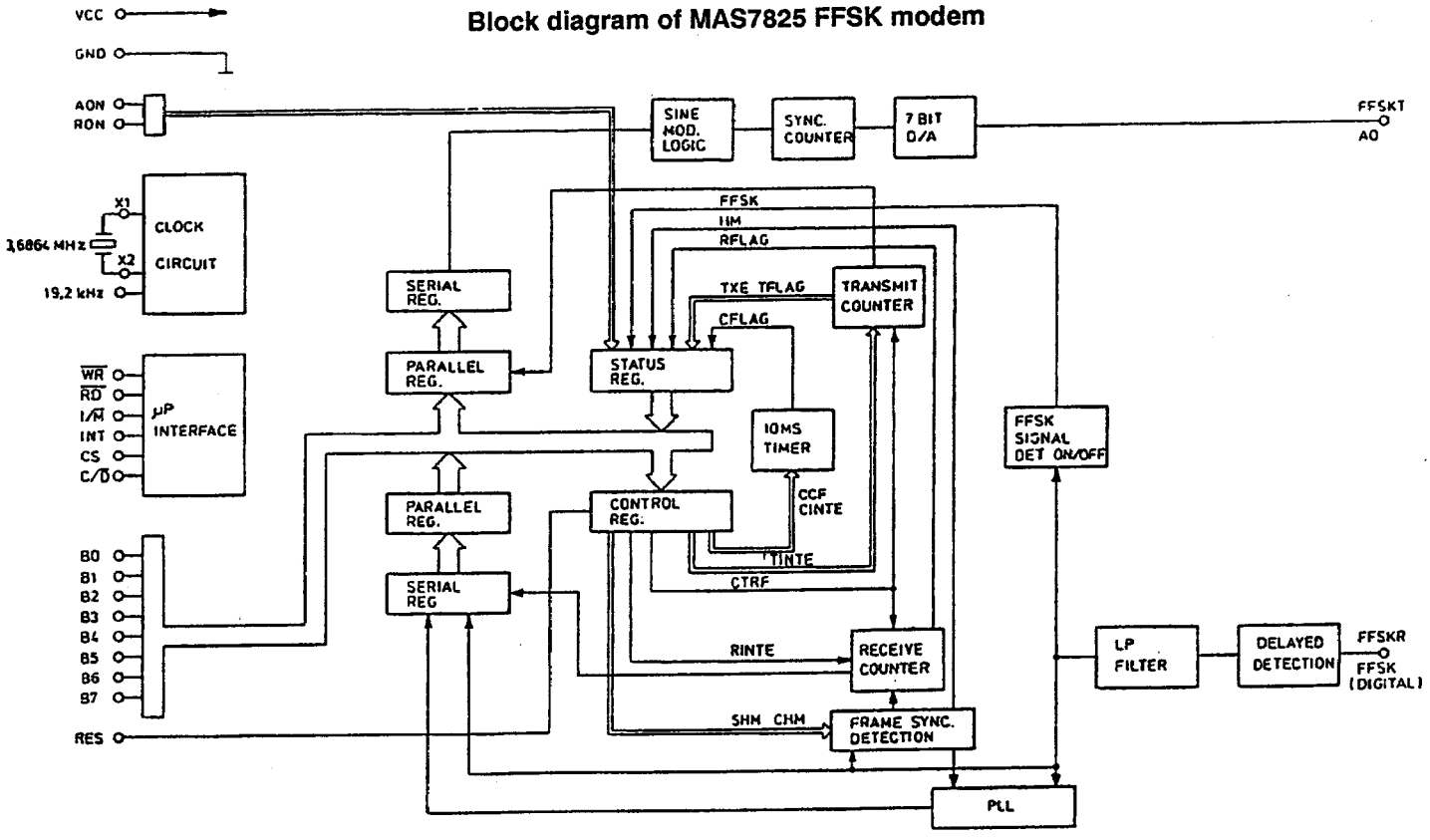
Block diagram of MAS7825 FFSK modem



Pin Description

Pin	Name	Type	Signal description	Pin	Name	Type	Signal description
1	OSC OUT		XTAL 3,6864 MHz	16	RES	DI	Clears the following flags: RFLAG, CFLAG, TXE, HM, SFR, RINTE, TINTE, CINTE and sets TFLAG (active high)
2	OSC IN		XTAL or external clock				
3	RD0	DI	Test input, connect to V_{SS} or V_{DD}				
4	M2	DI	Test input with pull up resistor				
5	$\overline{RD}$	DI	READ signal. Transfers data from the Tx-register or control register to the data bus depending on the state of the C/D-signal	20	RON	DI	External input for the status register, B7
				21	AON	DI	External input for the status register, B6
6	$\overline{WR}$	DI	WRITE signal. Transfers data to the Tx-register or to the control register depending on the state of the C/D-signal	22	RXC0	DI	Test input, connect to V_{SS} or V_{DD}
				23	19 K2	D0	Output clock 19,2 kHz
				24	TXC0	DI	Test input, connect to V_{SS} or V_{DD}
				25	I/M	DI	Intel/Motorola. Adaption for the Intel or the Motorola uP interface
7	C/$\overline{D}$	DI	Control/Data-signal. Selects the control and status register or the Rx- and Tx-register	26	INT	D0	Interrupt to uP (active high with I/$\overline{M}$ = high, active low with I/$\overline{M}$ = low)
8	CS	DI	Chip select (active high)				
9-13	B7-B3	DI/O	Bus for Tx-data, Rx-data, control and status	27	FFSK	DI	Demodulator input (logical, squarred FFSK signal)
17-19	B2-B0	DI/O					
14	V_{SS}	-	Negative supply voltage (0 V)	28	V_{DD}	-	Positive supply voltage (5 V typ)
15	AO	AO	Analog output signal from the modem				

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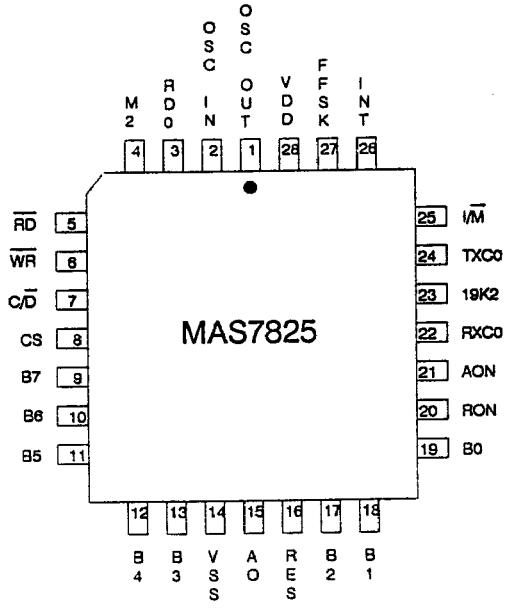
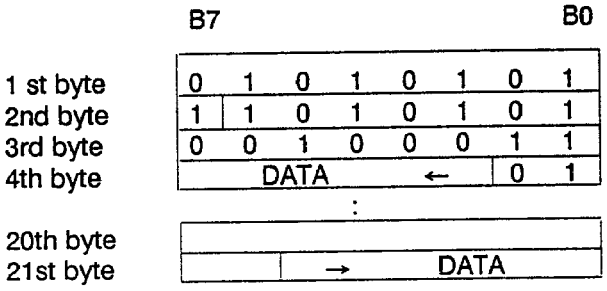
PIN CONFIGURATION 28 PIN PLCC



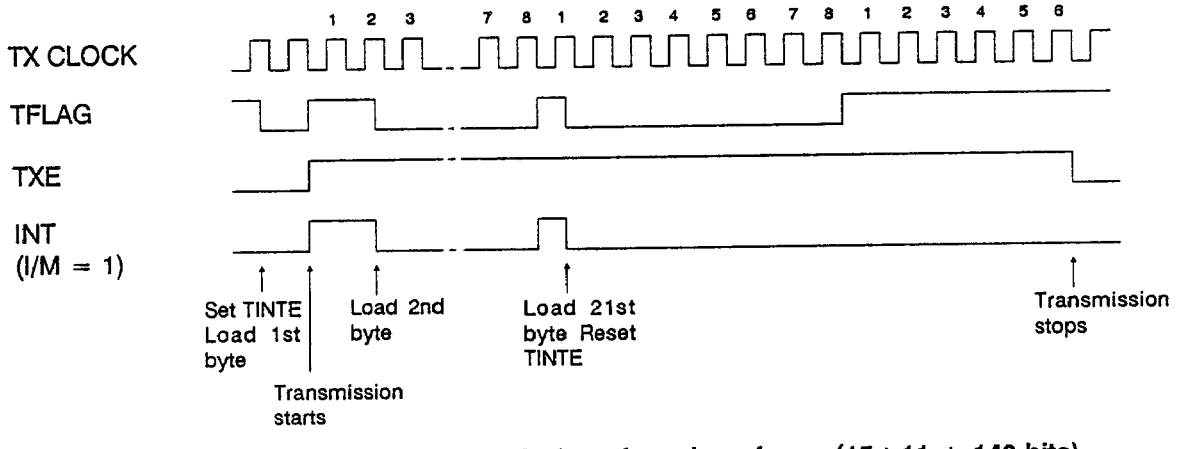
MODEM DATA TRANSFER

Data transmission



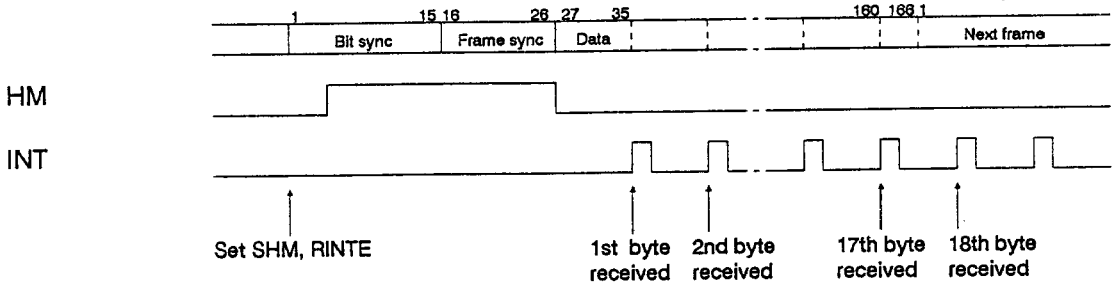
B0: the first bit sync bit
B7: the first frame sync bit

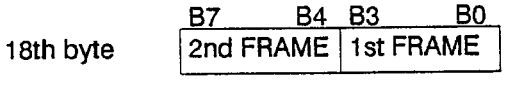
B5: the last data bit (166th) of transmitted frame



Transmission of one long frame (15+11 + 140 bits)

Data Reception





B3: last bit of the 1st frame = 140th received bit
B4: first bit of the second frame

MODEM CONTROL

Microprocessor interface

CS	C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	I/$\overline{M}$	Operation
0	X	X	X	X	Disabled
1	0	0	1	1	Read Rx - Register
1	1	0	1	1	Read Status Register
1	1	1	0	1	Write Control Register
1	0	1	0	1	Write Tx-Register
1	0	1	0	0	Read Rx-Register
1	1	1	0	0	Read Status Register
1	1	0	1	0	Write Control Register
1	0	0	1	0	Write Tx-Register

I/M = HIGH: Intel mode, INT = active high
I/M = LOW: Motorola mode, INT = active low

Control register

B7	B6	B5	B4	B3	B2	B1	B0

(All bits active HIGH)

B0	RINTE	Receiver interrupt enable control bit
B1	TINTE	Transmitter interrupt enable control bit
B2	CINTE	Timer (10 ms) interrupt enable control bit
B3	SFR	Short frame (106 bit) transmission enable bit
B4	SHM	Set hunt mode on. The modem is searching for the frame sync pattern IIIOOOIOOIO. RFLAG is kept LOW until first data byte is received.
B5	CHM	Clears hunt mode
B6	CCF	Clears timer interrput flag

Status register

B7	B6	B5	B4	B3	B2	B1	B0

(All bits active HIGH exept $\overline{FFSK}$)

B0	RFLAG	Received data interrupt flag. Flag is cleared when the receiver register is read.
B1	HM	Hunt for frame synchronization pattern IIIOOOIOOIO activated. Bit is cleared when frame Sync pattern received.
B2	TFLAG	Transmitter buffer empty enterrupt flag. Flag is cleared when the next byte is loaded into the tranmitter register. When tansmission is OFF, TFLAG is set.
B3	TXE	Transmission enable flag is set when transmission starts and is cleared when transmission ends.
B4	$\overline{FFSK}$	FFSK signal is detected when bit cleared
B5	CFLAG	10 ms timer interrupt flag
B6	AON	External input from pin AON

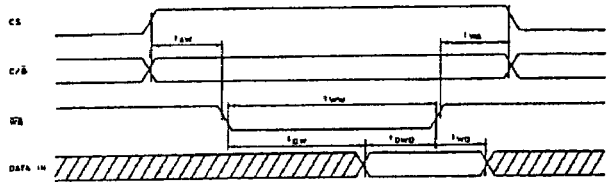
Analog Characteristics

	Symbol	Min	Typ	Max	Unit	Condition
Output level	VAO	2,9	3,2	3,5	VPP	V_{DD} = +5 V
Output DC-level (Sine wave)	VAODC	2,3	2,5	2,7	V	V_{DD} = +5 V
Output impedance	ZO	17	25	32	k	
Output frequency MARK	fM	1180	1200	1220	Hz	fXTAL =
Output frequency SPACE	fS	1780	1800	1820	Hz	3,6864 MHz
Output distortion	DO			-42	dB	

Timing diagrams
Intel mode

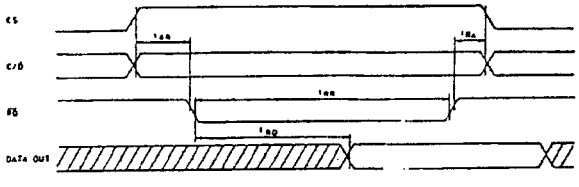
Write

$t_{AW} > 0$, $t_{WA} > 0$

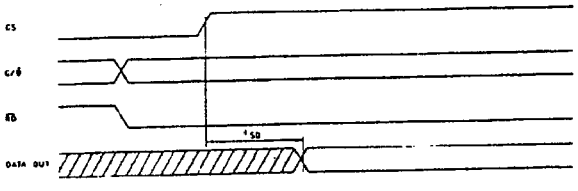


Read

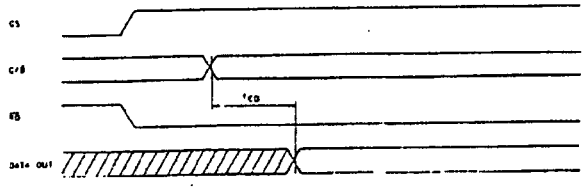
t_{AR} = 30 ns, $t_{RA} > 0$



Read

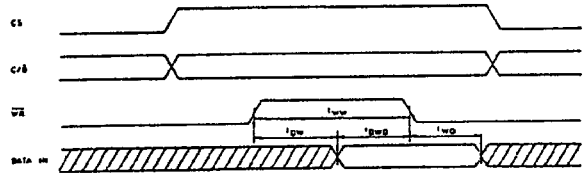


Read

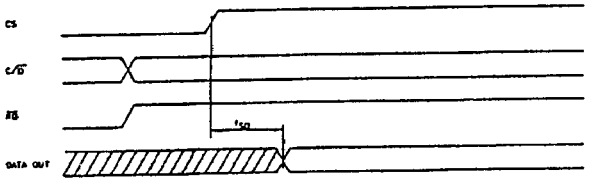


Motorola mode

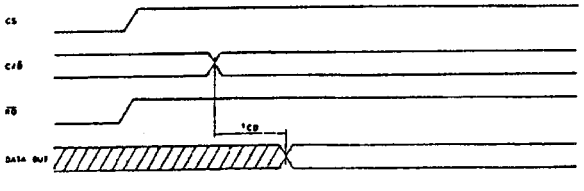
Write



Read



Read



ELECTRICAL CHARACTERICTICS

Absolute maximum ratings

Supply voltage	V_{DD}	-0,3 to 6,2 V
Input voltage (any pin)	VIN	-0,3 V to V_{DD} + 0,3 V
Operating temperature	TA	-25 °C to + 70 °C
Storage temperature		-55 °C to + 125 °C

DC characteristics

V_{DD} = 5 V ± 5 % TA = -25 °C... + 70 °C

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Supply current	IDO		2	5	mA	
Input low voltage	VIL			0,8	V	Digital inputs
Input high	VIH	2,7			V	except OSC IN
Input low voltage OSC IN	VIL			0,5	V	If external
Input high voltage OSC IN	VIH	4,0			V	clock used
Output low voltage	VOL			0,4	V	IOL = 2,5 mA
Output high voltage	VOH	3,0			V	IOH = -1 mA
Input leakage current	ILI	-1		1	µA	

AC Characteristics

V_{DD} = 5 V ± 5 % TA = -25 °C... + 70 °C R_L = 10 kohm C_L = 50 pF

INTEL mode I/$\overline{M}$ = high MOTOROLA mode I/$\overline{M}$ = low

Parameter	Symbol	Min	Typ	Max	Unit	Condition
$\overline{WR}$ pulse width	TWW	100			ns	
Data set up before $\overline{WR}$	tDWD	50			ns	
Input data from $\overline{WR}$	tDW			50	ns	
Data hold from $\overline{WR}$	tDW	50			ns	
$\overline{RD}$ pulse width	tRR	170			ns	
Access time from RD	tRD			150	ns	
Access time from CS	tSD			150	ns	
Access time from C/D	tCD			180	ns	